ABSTRACT

As shown in FIG. 1, an operation-processing device of the present invention comprises a register array (11) having plural registers for holding an arbitrary value based on a write address Aw and a write control signal Sw and outputting this value based on a read address Ar, an ALU (12) for performing operations on this value, a decoder (13) for decoding an operation instruction from an operation program AP for operating this ALU (12), and an instruction-execution-controlling portion (50) for controlling the register array (11) and the ALU (12) in order to execute this operation instruction, wherein this instruction-execution-controlling portion (50) selects one of the registers based on the operation instruction and performs register-to-register addressing processing that, based on a value held by this selected register, selects another register.